

Abstract of the Disclosure

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A multiply-accumulate circuit includes a compressor tree to generate a product with a binary exponent and a mantissa in carry-save format. The product is converted into a number having a three bit exponent and a fifty-seven bit mantissa in carry-save format for accumulation. An adder circuit accumulates the converted products in carry-save format. The adder operates on floating point number representations having exponents with a least significant bit weight of thirty-two, and exponent comparisons within the adder exponent path are limited in size. The adder circuit includes intermediate registers to provide multi-threaded capability. Products interleaved in time are accumulated into separate sums simultaneously.